

Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the Application.

Listing of Claims:

1. (Original) A method for determining overlay tolerance for a lot of semiconductor wafers comprising:

measuring a first patterned layer on some of said semiconductor wafers so as to obtain a first set of critical dimension error measurements;

measuring a second patterned layer on some of semiconductor wafers so as to obtain a second set of critical dimension error measurements; and

determining overlay tolerance for said lot of semiconductor wafers using said first set of critical dimension error measurements, said second set of critical dimension error measurements and a line edge placement specification for said lot of semiconductor wafers.

2. (Original) The method of Claim 1 wherein said measuring a first patterned layer further comprises:

selecting from said lot of semiconductor wafers a first set of sample wafers; and

measuring critical dimension error at a plurality of locations on each semiconductor wafer in said first set of sample wafers.